FIG. 1

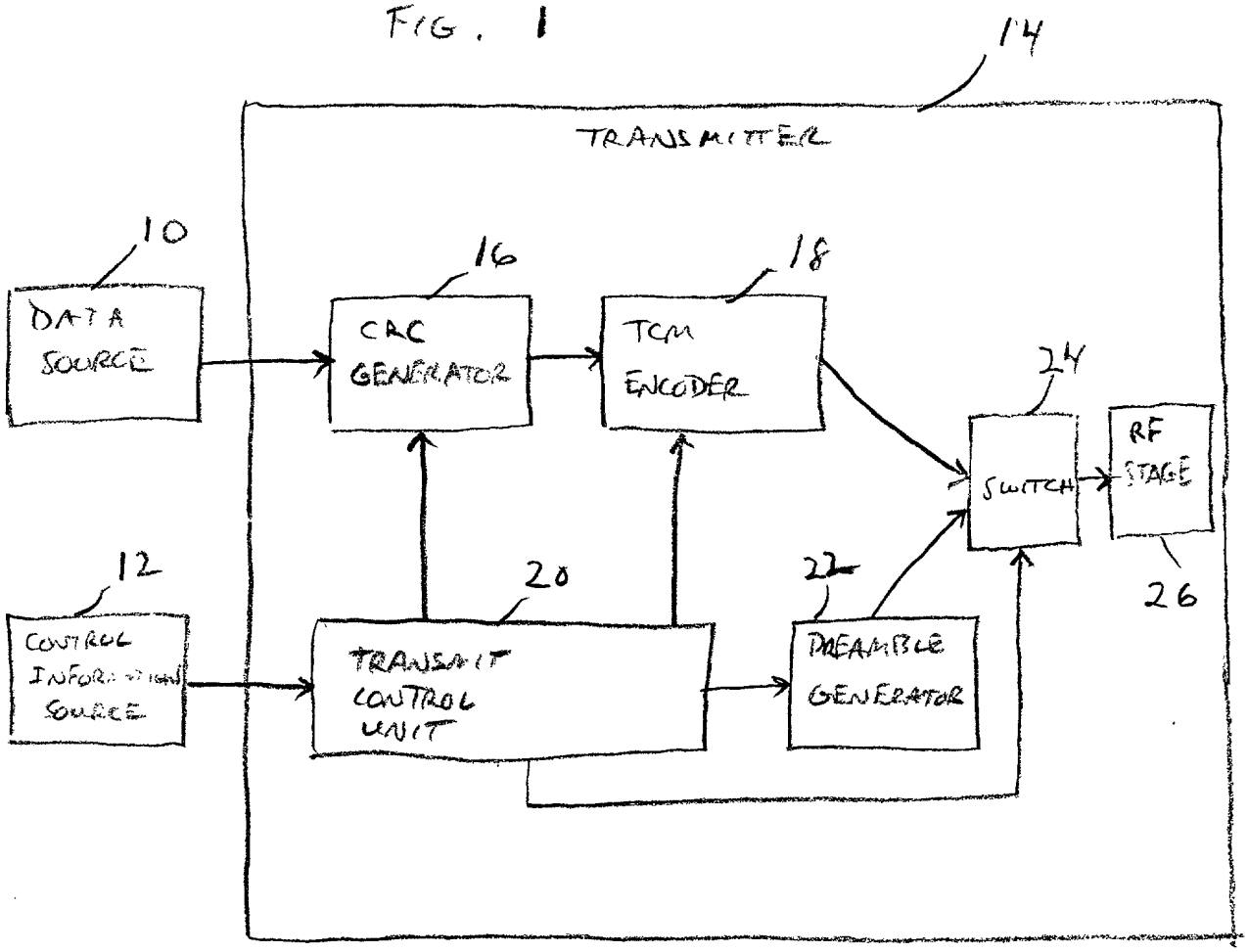

14
TRANSMITTER
10
DATA SOURCE
16
CRC GENERATOR
18
TCM ENCODER
24
SWITCH
RF STAGE
26
12
CONTROL INFORMATION SOURCE
20
TRANSMIT CONTROL UNIT
22
PREAMBLE GENERATOR

FIG. 2

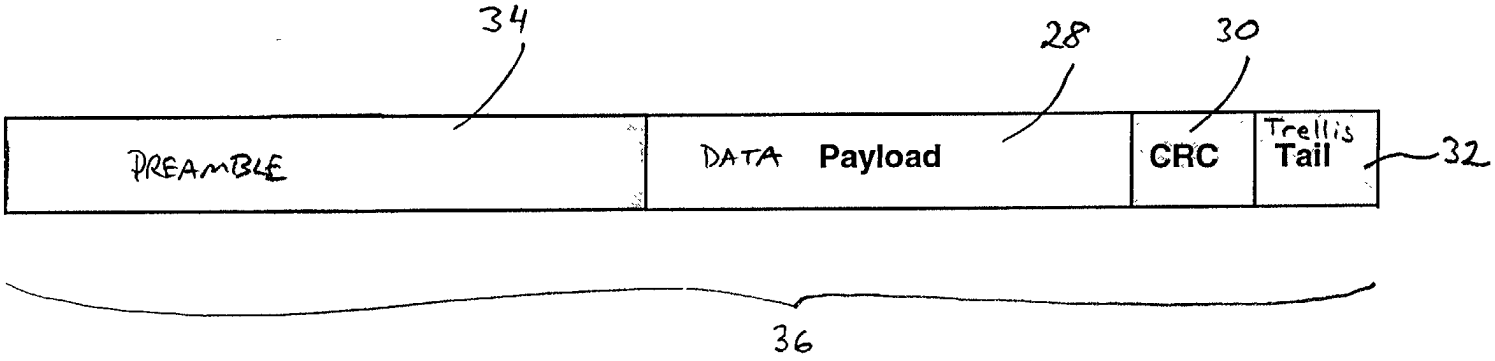


FIG. 3

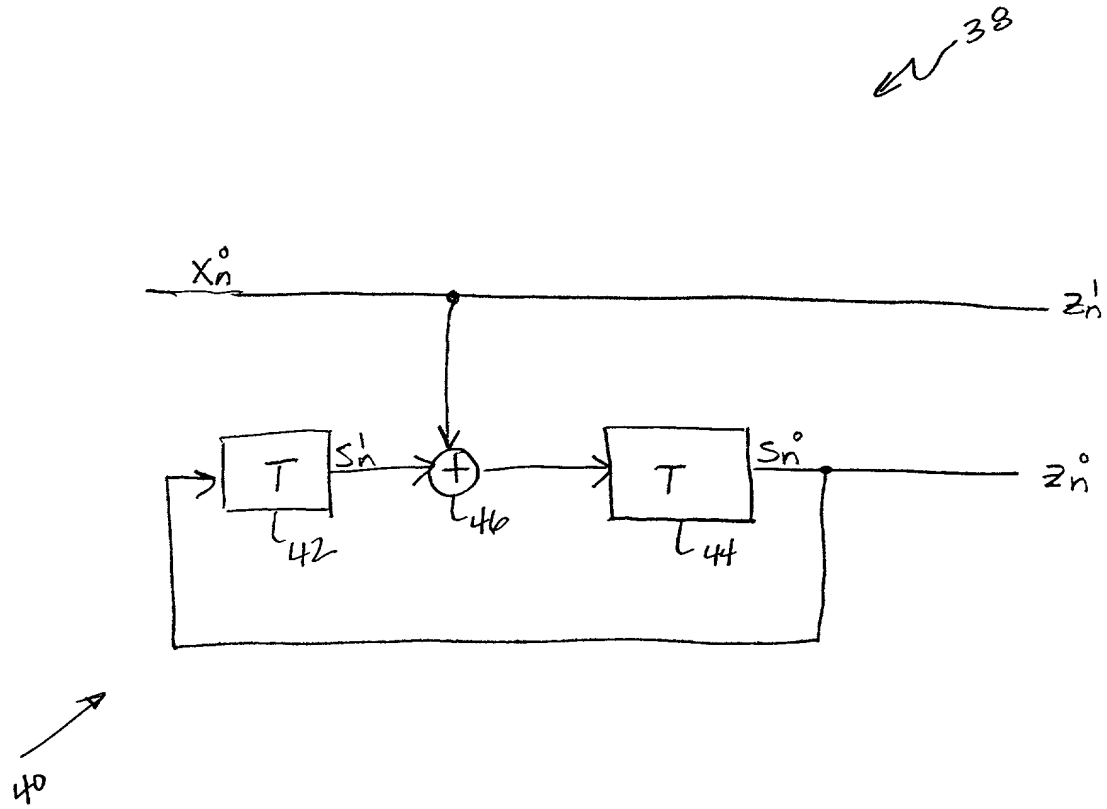


FIG. 4

Current State Bits s_n^1 s_n^0 (50)	Input Signal Bits x_n^0 (52)	Output Signal Bits z_n^1 z_n^0 (54)	Next State Bits s_{n+1}^1 s_{n+1}^0 (56)
0 0	0	0 0	0 0
	1	1 0	0 1
0 1	0	0 1	1 0
	1	1 1	1 1
1 0	0	0 0	0 1
	1	1 0	0 0
1 1	0	0 1	1 1
	1	1 1	1 0

FIG. 5

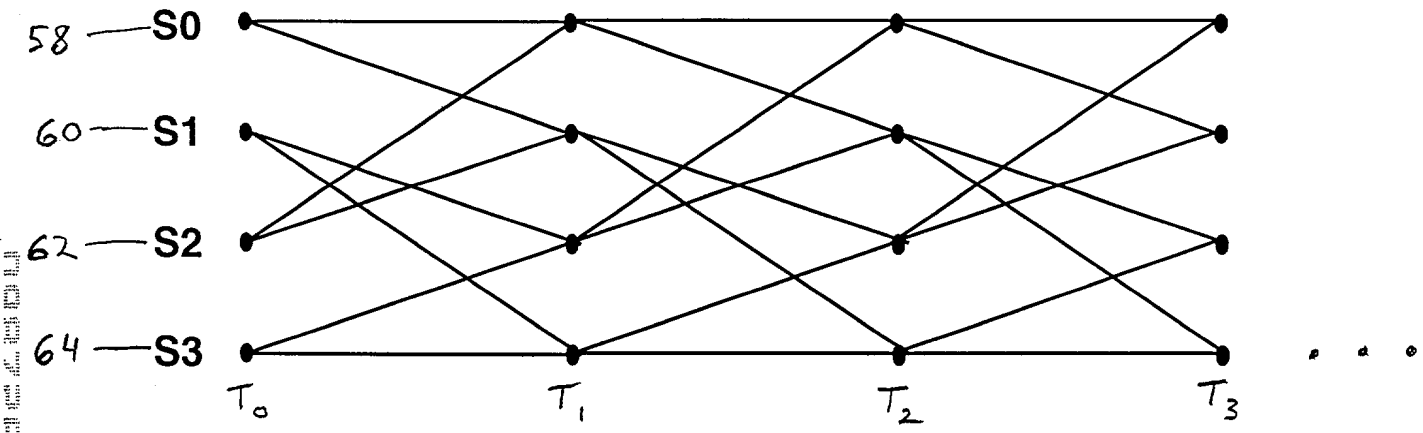

58
S0
60
S1
62
S2
64
S3
T0
T1
T2
T3

FIG. 9

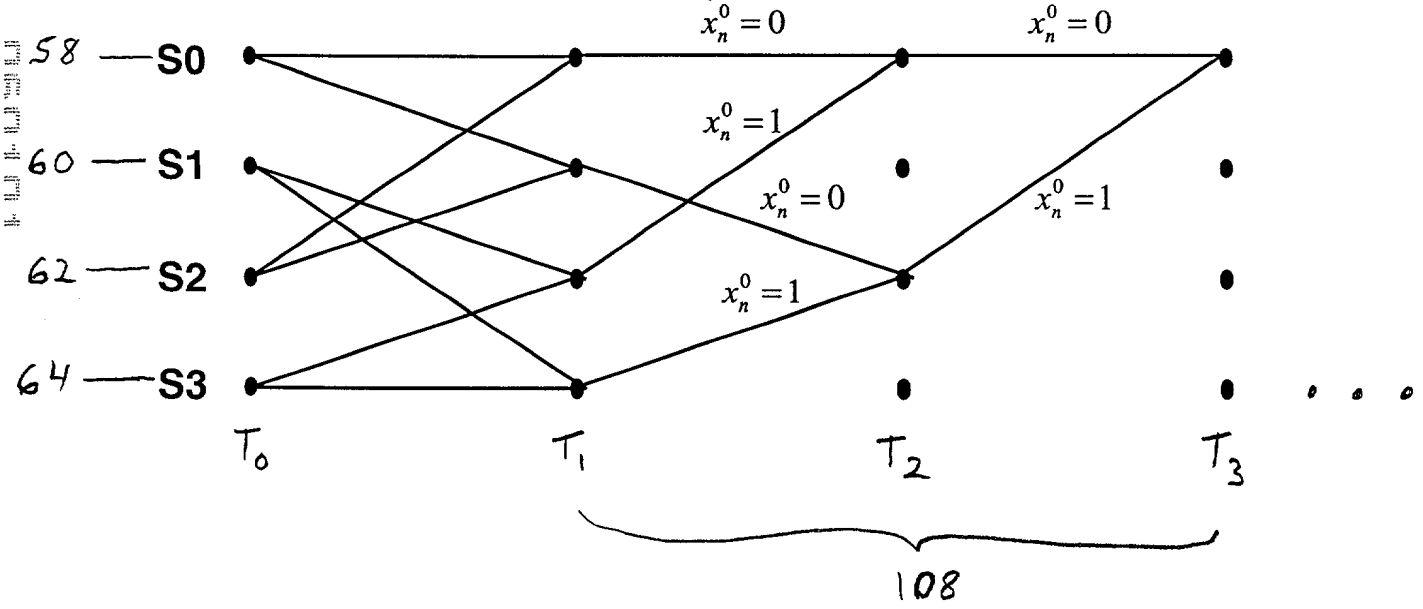

58
S0
60
S1
62
S2
64
S3
$x_n^0 = 0$
$x_n^0 = 0$
$x_n^0 = 1$
$x_n^0 = 0$
$x_n^0 = 1$
$x_n^0 = 1$
T0
T1
T2
T3
108

FIG. 6

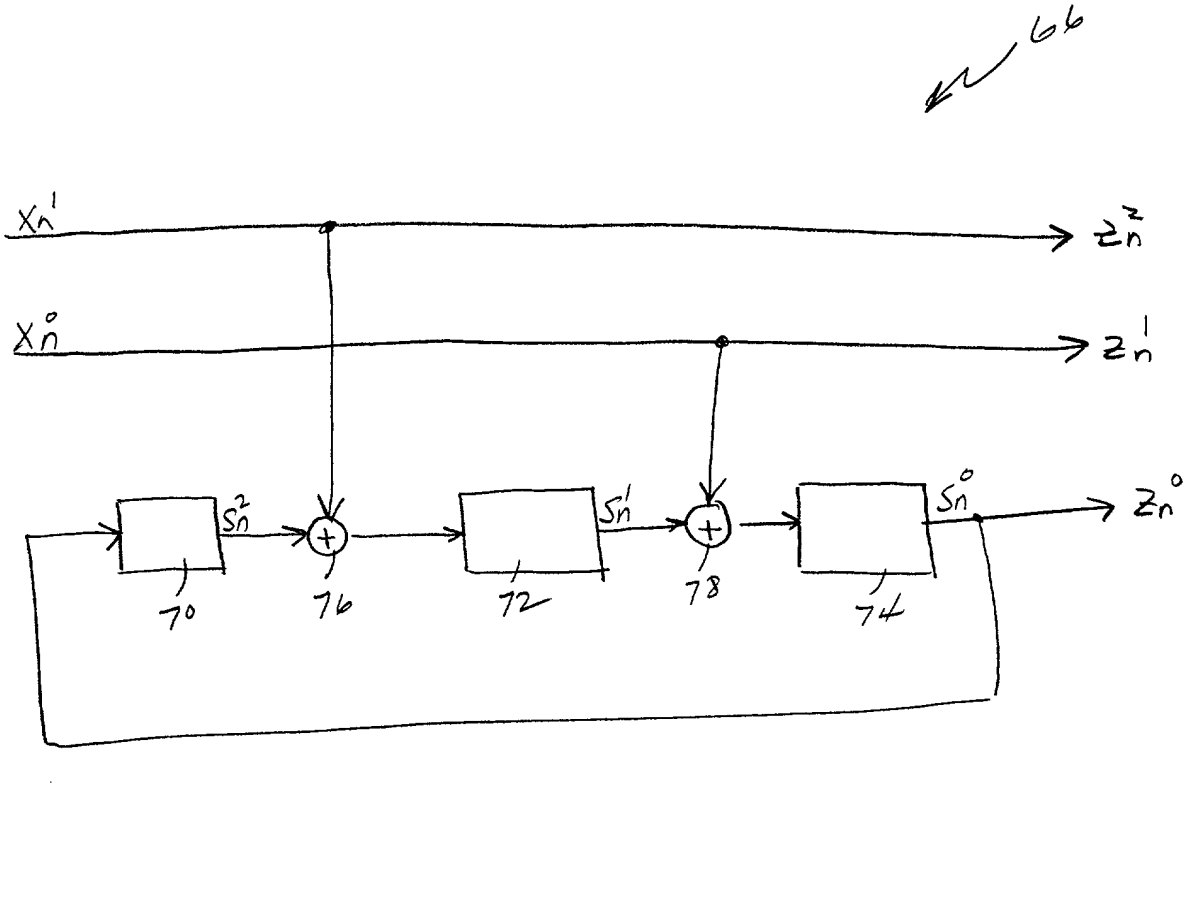


FIG. 7

Current State Bits s_n^2 s_n^1 s_n^0 (84)	Input Signal Bits (86) x_n^1 x_n^0	Output Signal Bits (88) z_n^2 z_n^1 z_n^0	Next State Bits (90) s_{n+1}^2 s_{n+1}^1 s_{n+1}^0
0 0 0	0 0	0 0 0	0 0 0
	0 1	0 1 0	0 0 1
	1 0	1 0 0	0 1 0
	1 1	1 1 0	0 1 1
0 0 1	0 0	0 0 1	1 0 0
	0 1	0 1 1	1 0 1
	1 0	1 0 1	1 1 0
	1 1	1 1 1	1 1 1
0 1 0	0 0	0 0 0	0 0 1
	0 1	0 1 0	0 0 0
	1 0	1 0 0	0 1 1
	1 1	1 1 0	0 1 0
0 1 1	0 0	0 0 1	1 0 1
	0 1	0 1 1	1 0 0
	1 0	1 0 1	1 1 1
	1 1	1 1 1	1 1 0
1 0 0	0 0	0 0 0	0 1 0
	0 1	0 1 0	0 1 1
	1 0	1 0 0	0 0 0
	1 1	1 1 0	0 0 1
1 0 1	0 0	0 0 1	1 1 0
	0 1	0 1 1	1 1 1
	1 0	1 0 1	1 0 0
	1 1	1 1 1	1 0 1
1 1 0	0 0	0 0 0	0 1 1
	0 1	0 1 0	0 1 0
	1 0	1 0 0	0 0 1
	1 1	1 1 0	0 0 0
1 1 1	0 0	0 0 1	1 1 1
	0 1	0 1 1	1 1 0
	1 0	1 0 1	1 0 1
	1 1	1 1 1	1 0 0

FIG. 8

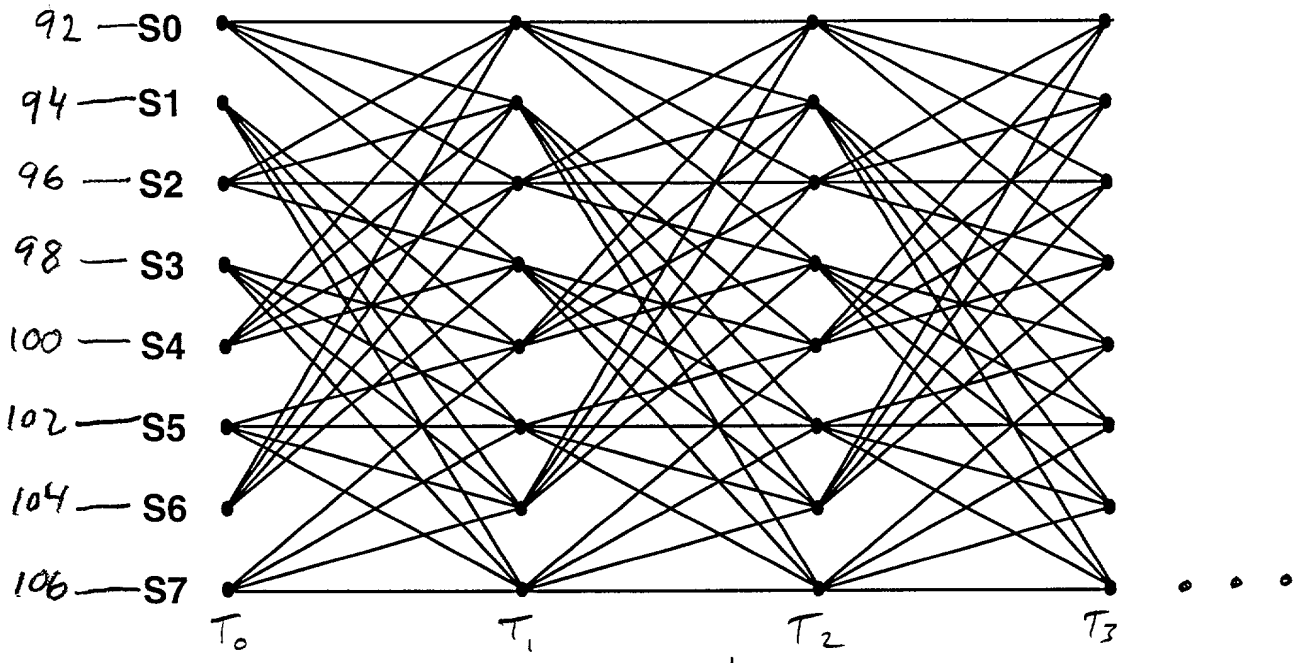

92 — S0
94 — S1
96 — S2
98 — S3
100 — S4
102 — S5
104 — S6
106 — S7
T_0
T_1
T_2
T_3

FIG. 14

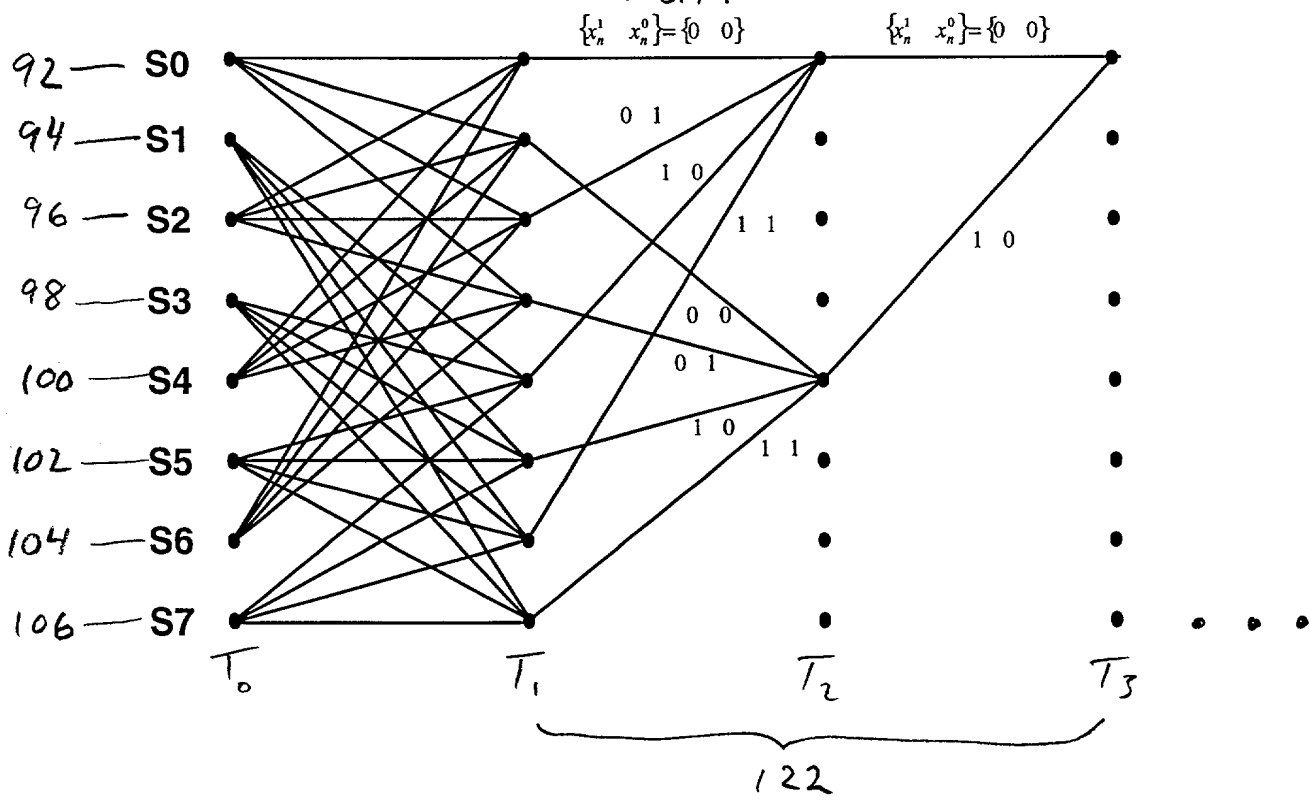

$\{x_n^1 \; x_n^0\} = \{0 \; 0\}$
$\{x_n^1 \; x_n^0\} = \{0 \; 0\}$
92 — S0
94 — S1
96 — S2
98 — S3
100 — S4
102 — S5
104 — S6
106 — S7
0 1
1 0
1 1
0 0
0 1
1 0
1 1
1 0
T_0
T_1
T_2
T_3
122

FIG. 10

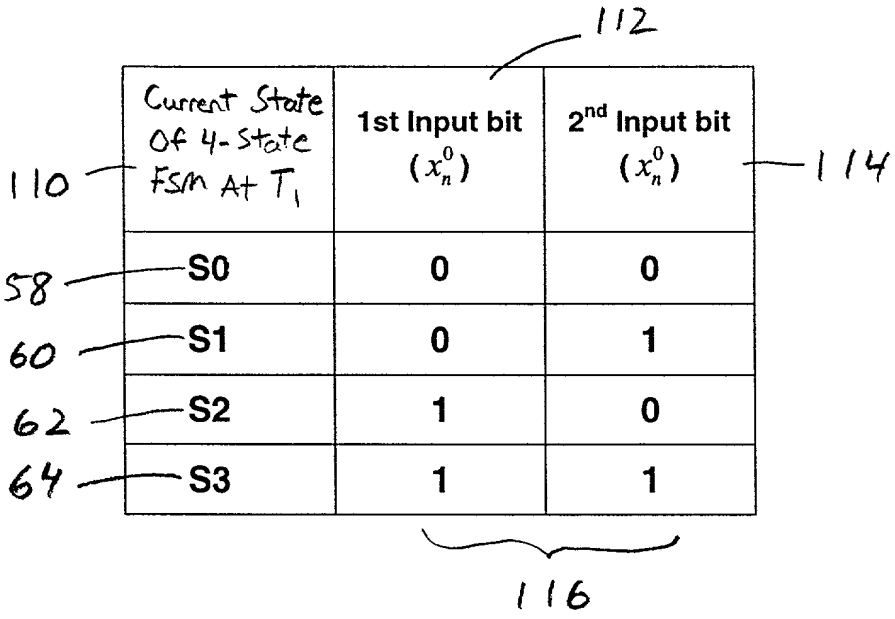

112
Current State Of 4-State FSM At T_1
1st Input bit (x_n^0)
2nd Input bit (x_n^0)
110
114
58
S0
0
0
60
S1
0
1
62
S2
1
0
64
S3
1
1
116

FIG. 11

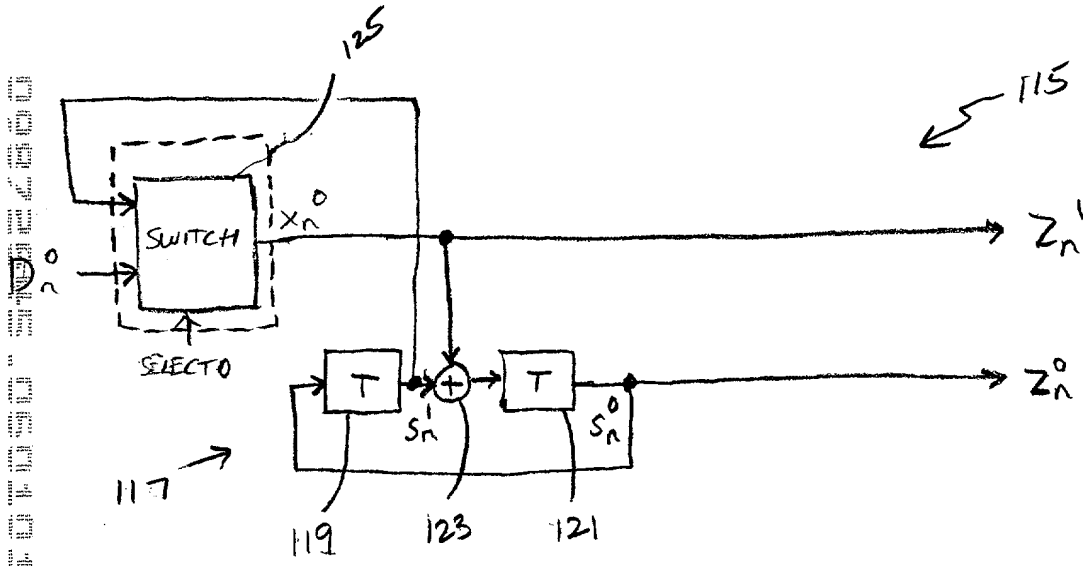

125
115
SWITCH
X_n^0
D_n^0
Z_n^1
Z_n^0
SELECTO
T
T
S_n^1
S_n^0
117
119
123
121

FIG. 12

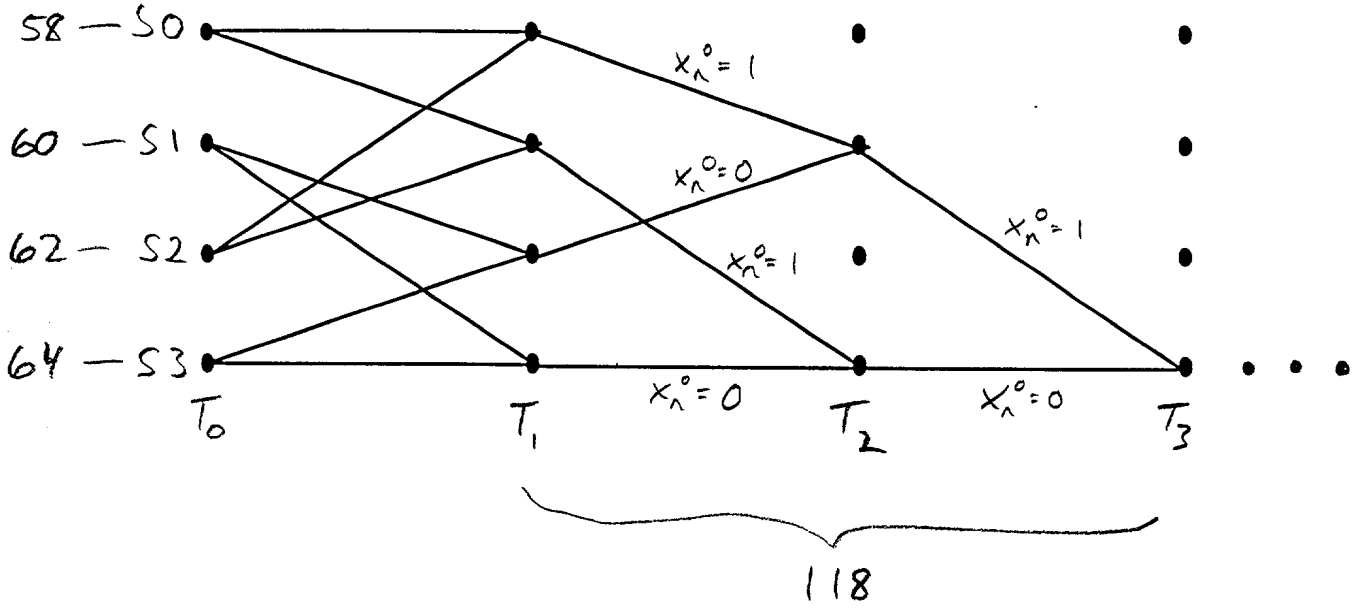

58 — S0
60 — S1
62 — S2
64 — S3
T_0
T_1
T_2
T_3
$x_n^0 = 1$
$x_n^0 = 0$
$x_n^0 = 1$
$x_n^0 = 1$
$x_n^0 = 0$
$x_n^0 = 0$
118

FIG. 13

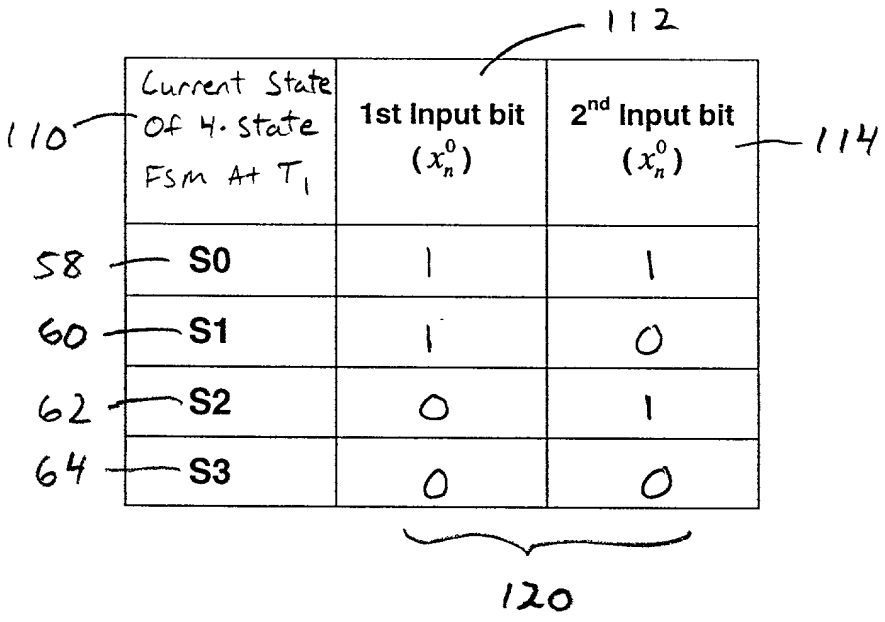

112
110
Current State Of 4-State FSM At T_1
1st Input bit (x_n^0)
2nd Input bit (x_n^0)
114
58
S0
1
1
60
S1
1
0
62
S2
0
1
64
S3
0
0
120

FIG. 15

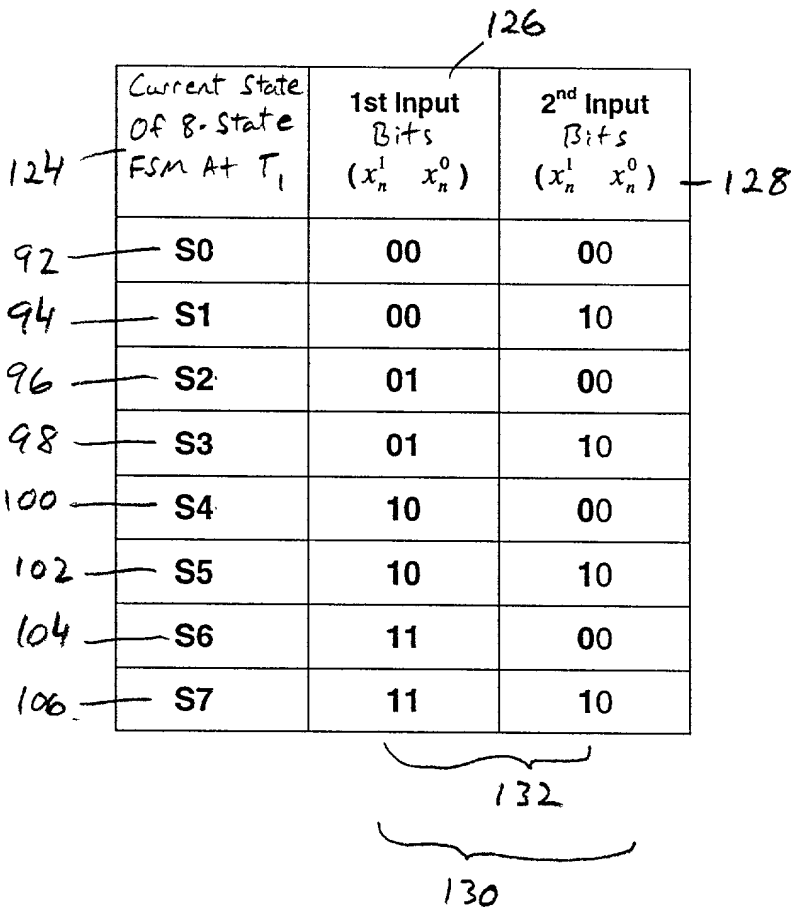

126
Current State Of 8-State FSM At T_1
1st Input Bits (x_n^1 x_n^0)
2nd Input Bits (x_n^1 x_n^0)
124
128
92 S0 00 00
94 S1 00 10
96 S2 01 00
98 S3 01 10
100 S4 10 00
102 S5 10 10
104 S6 11 00
106 S7 11 10
132
130

FIG. 16

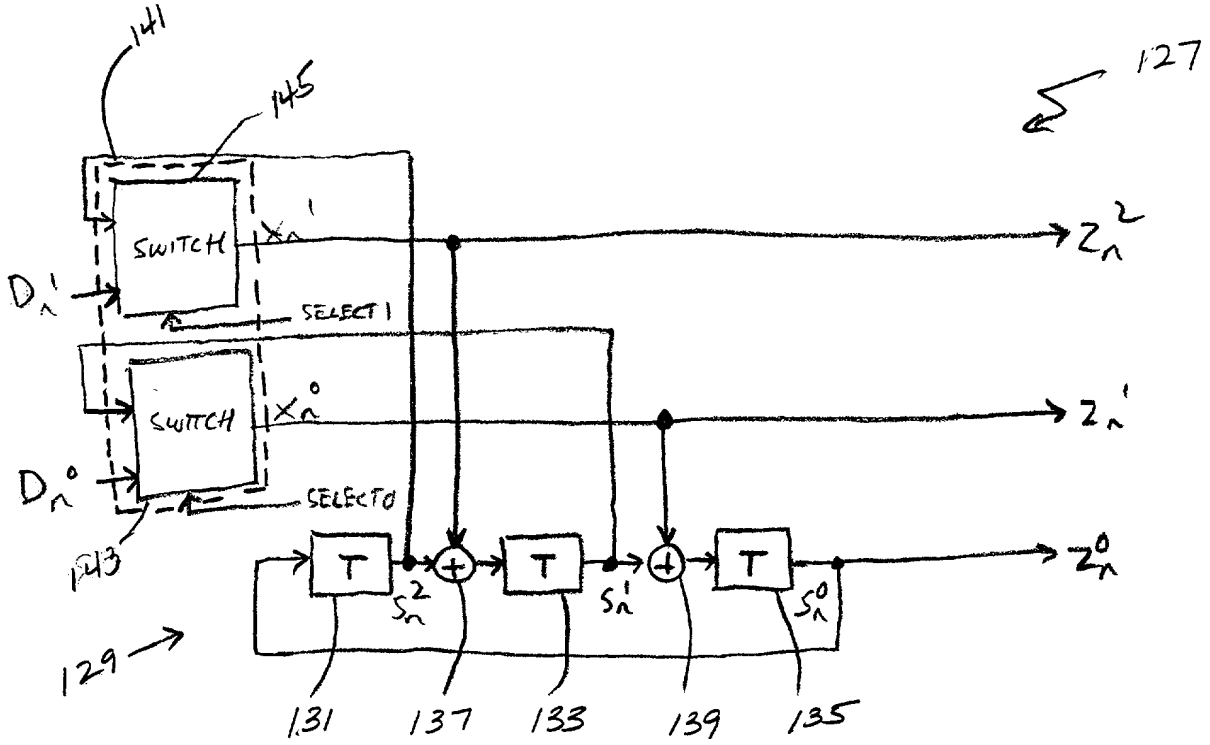

141
145
127
SWITCH
SELECT 1
SWITCH
SELECT 0
143
T
T
T
129
131
137
133
139
135

FIG. 17

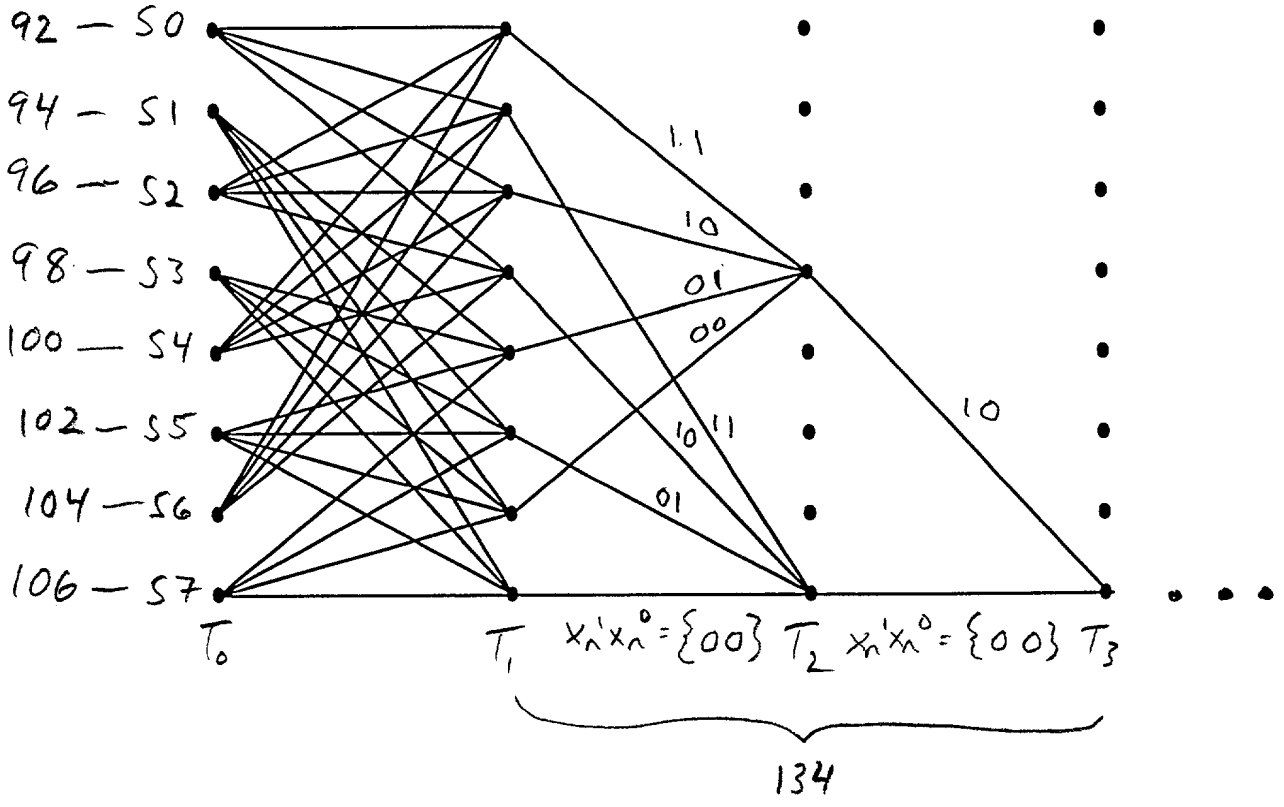
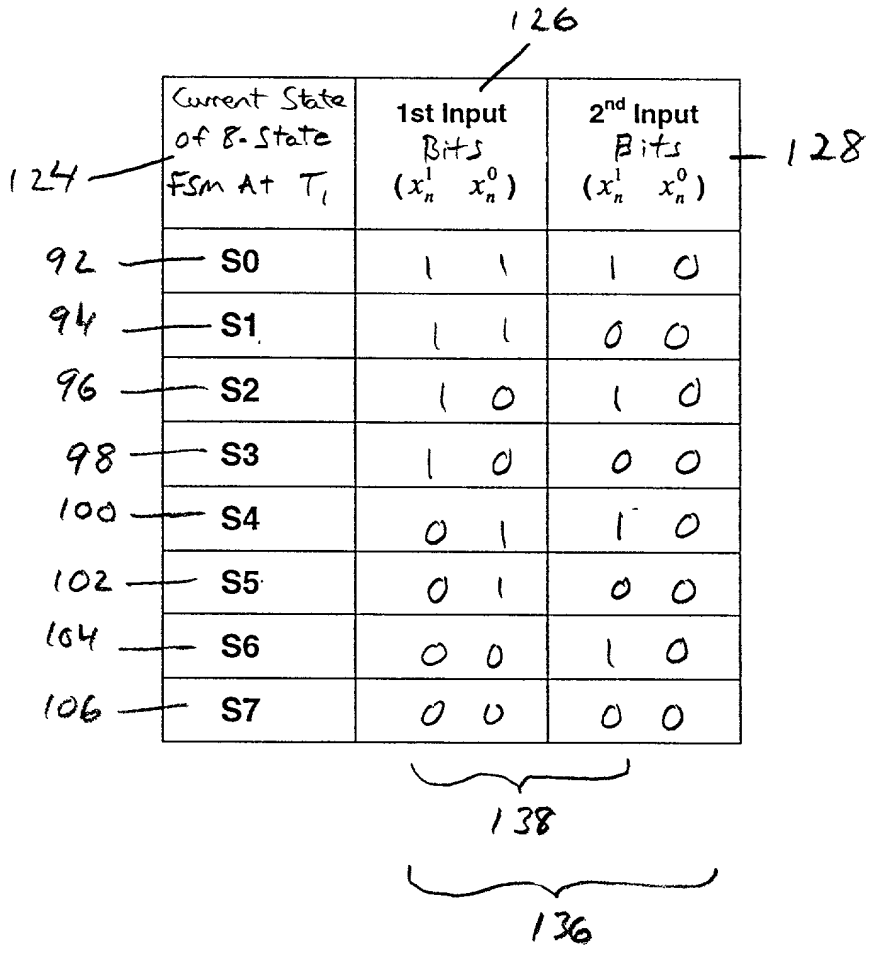

92 — S0
94 — S1
96 — S2
98 — S3
100 — S4
102 — S5
104 — S6
106 — S7
1.1
10
01
00
10
11
01
10
T0
T1
$x_n' x_n^0 = \{00\}$
T2
$x_n' x_n^0 = \{00\}$
T3
134

FIG. 18


126
Current State of 8-State FSM At T_1
1st Input Bits (x_n^1 x_n^0)
2nd Input Bits (x_n^1 x_n^0)
128
124
92
S0
1 1 1 0
94
S1
1 1 0 0
96
S2
1 0 1 0
98
S3
1 0 0 0
100
S4
0 1 1 0
102
S5
0 1 0 0
104
S6
0 0 1 0
106
S7
0 0 0 0
138
136